REMARKS

This application has been reviewed in light of the Office Action dated September 17, 2008.

Claims 1-22 are in the application; claims 13-20 have been withdrawn from consideration by the Examiner. Claims 1-12, 21 and 22 are presented for examination. Claim 1 has been amended. Claims 21 and 22 have been added Claim 1 and claim 13 (withdrawn) are independent. Favorable review is respectfully requested.

The drawings have been amended by submission of three (3) replacement sheets, each labeled "Replacement Sheet" as required by 37 C.F.R. § 1.121(d). The first two replacement sheets (numbered "1/5" and "2/5") present FIGS. 1-4 in numerical order. No change to the content of these figures has been made. In the third replacement sheet, numbered "4/5", FIG. 7 has been amended to show molding compound 36 in the gaps underneath semiconductor device 28 (compare with the open gaps shown in FIG. 6B). This is consistent with the discussion of the figure in the specification at page 7, lines 22-23, which clearly states that the compound encapsulates the device. Accordingly, no new matter has been added. FIG. 7 has also been amended to correct reference numeral "29", which does not appear in the specification, to "24". The specification has been amended by replacing the paragraph on page 7, lines 12-21, to delete a reference to a "preferable" spacing between the semiconductor device and the routing circuits. The revised sentence in this paragraph states that the spacing 32 between the semiconductor device 28 and routing circuits 26 is to facilitate the flow of a second molding compound. Originally filed claim 6 specifies that the spacing distance 32 is at least 75 microns. New claim 22 specifies that this spacing is at least 25 microns.

New claim 21 explicitly recites that the chip attach sites (24) are not coplanar with the routing circuits (26). This feature is supported in the specification by FIGS. 4 and 6B and the accompanying discussion of those figures. Claim 1 does not have a requirement regarding the chip attach sites being planar or coplanar with the routing circuits; dependent claim 21 specifies that the chip attach sites and routing circuits are not coplanar.

Claim 1, the only independent claim now under consideration, has been amended to explicitly recite a package including a lead frame formed from an electrically conductive substrate. The lead frame has opposing first and second ends. The second ends terminate at an

array of chip attach sites directly electrically interconnected by interconnections to input/output pads on a semiconductor device; the chip attach sites are disposed opposite the input/output pads. Support for this amended claim language appears in the specification at least at page 5, lines 31-32, and page 7, lines 1-15, with reference to FIGS. 4, 6A and 6B.

Claims 1-5 and 9-12 were rejected under 35 U.S.C. § 103(a) as unpatentable over Choi (U.S. Pat. Application Publication No. 2002/0105077) in view of Kuo et al. (U.S. Pat. Application Publication No. 2002/0197842). The applicants respectfully submit that amended independent claim 1 is patentably distinct from the cited art, for the following reasons.

Claim 1 has been amended to recite that the substrate is electrically conductive, and that and that the chip attach sites are disposed opposite the input/output pads of the device. This is consistent with a "flip chip" approach, the details of which are discussed in the specification. Choi is understood to disclose a semiconductor package using wirebond sites, as opposed to a flip chip arrangement with an array of chip attach sites. Furthermore, in the conventional package pointed out by the Examiner (Choi, FIG. 1), the substrate 10 is an insulator (see Choi, paragraph [0008]). Choi clearly is concerned with a different packaging scheme from the present invention, and does not suggest a conductive substrate or chip attach sites opposite input/output pads of a device. Kuo et al. is understood to discloses a method for forming solder bumps; Kuo et al. does not suggest a conductive substrate for a package, and does not remedy the defects of Choi as a reference against amended claim 1. It therefore is submitted that independent claim 1 is not rendered obvious by the cited references, considered either singly or in combination.

Claims 6 and 7, dependent from claim 1, were rejected as obvious from the combination of Choi and Kuo et al. with Shimanuki et al (U.S. Pat. Application Publication No. 2002/0168796); claim 8, dependent from claim 1, was rejected as obvious from the combination of Choi and Kuo et al. with Sakamoto et al. (U.S. Pat. No. 6,967,401). The applicants wish to point out that neither Shimanuki et al. nor Sakamoto et al. is concerned with a flip-chip arrangement; in particular, neither of these references suggests an array of chip attach sites opposite the input/output pads of a device. Accordingly, neither of these references, even when considered in combination with Choi and Kuo, renders obvious the package of independent claim 1.

The other claims now under consideration are dependent from the independent claim discussed above and are believed to be patentable for the same reasons. Since each dependent claim is directed to a separate aspect of the invention, however, the individual consideration of each claim on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, favorable consideration and early passage to issue of the application are respectfully requested.

The applicants' undersigned attorney may be reached by telephone at 212-551-2625. All correspondence should continue to be directed to the address given below, which is the address associated with Customer Number 27267.

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